**module mod22Cntr(O, ck, rst);**

**input ck, rst;**

**output [4:0] O;**

**reg [4:0] O;**

**always @ (posedge ck)**

**if (~rst)**

**if (O == 5'd21)**

**O <= 5'd0;**

**else**

**O <= O+1;**

**always @ (posedge rst)**

**O <= 5'd0;**

**endmodule**

**module test\_mod22Cntr;**

**reg clock;**

**reg reset;**

**wire[4:0] out;**

**mod22Cntr c1 (.ck(clock), .rst(reset), .O(out));**

**always**

**#5 clock = ~clock;**

**initial**

**begin**

**clock = 1'b0;**

**reset = 1'b1;**

**#7**

**reset = 1'b0;**

**#400 $finish;**

**end**

**initial**

**$monitor($time, " Count = %b", out);**

**endmodule**

|  |  |
| --- | --- |
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